In the Claims:

1-12 (cancelled)

13. (original) A diode having a first and a second terminal, the diode comprising an n-MOS transistor having a channel, a first N+ doped diffusion region at one extremity of the channel and a second N+ diffusion region at the other extremity of the channel, and a p-MOS transistor having a channel and a first P+ doped diffusion region at one extremity of the channel and a second P+ diffusion region at the other extremity of the channel,

the first N+ diffusion region of the n-MOS transistor being coupled to the first P+ diffusion region of the p-MOS transistor,

the gate of the n-MOS transistor being coupled to the second P+ diffusion region of the p-MOS transistor, and the gate of the p-MOS transistor being coupled to the second N+ diffusion region of the n-MOS transistor, and

the second P+ diffusion region of the p-MOS transistor being coupled to the first terminal of the diode and the second N+ diffusion region of the n-MOS transistor being coupled to the second terminal of the diode,

a current versus voltage characteristic of the diode being such that it has a negative slope in a reverse biased state of the diode.

14. (original) A diode according to claim 13, whereby the current versus voltage characteristic of the diode substantially passes through the origin of the current voltage characteristic.

15. (original) Voltage doubler comprising two diodes coupled in series between a supply voltage node and an output node, the anode of the first diode being coupled to the supply voltage node, and the cathode of the second diode being coupled to the output node, a clock signal switching between a first and a second voltage level being applied to the node between the cathode of the first diode and the anode of the second diode, and a load capacitance being connected to the output node, whereby the two diodes are diodes according to any of claims 13 or 14.

16. (original) Memory cell comprising two ultra-low power diodes according to claim 13 coupled in series reversely biased between a first low voltage level and a second high voltage level, the voltage level of the memory cell being present at the node between the two ultra-low power diodes.

17. Use of the memory cell of claim 16 as a level holder in domino logic.

18. Use of the memory cell of claim 16 as a level restoring device in pass gate logic.

19. Use of the memory cell of claim 16 as a data storing device in a D latch.

20. Use of the memory cell of claim 16 to maintain information on high impedance floating nodes in digital circuits.

21. Use of the memory cell of claim 16 as a level keeper device in MTCMOS circuits.

22. Electrostatic discharge protection circuit comprising a first reverse biased diode between a node to be protected and a first power supply and a second reverse biased diode between the node to be protected and a second power supply, whereby the diodes are diodes according to claim 13.

23-25 (cancelled)